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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Official

In re Application of

Gerard Chauvel, et al.

Serial No.: **08/890,894**

Filed: **07/10/97**

TIF-15767A

Examiner: **D. Tran**

Art Unit: **2186**

Conf. No.: **5253**

For: **MULTIPLE PROCESSOR APPARATUS HAVING A PROTOCOL PROCESSOR INTENDED FOR THE EXECUTION OF A COLLECTION OF INSTRUCTIONS IN A REDUCED NUMBER OF OPERATIONS**

AMENDMENT - 37 C.F.R. § 1.111

Assistant Commissioner for Patents
Washington, D.C. 20231

MAILING CERTIFICATE UNDER 37 C.F.R. § 1.8(A)

I hereby certify that the above correspondence is being deposited with the U.S. Postal Serve as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, DC 20231.

Elizabeth Austin — Date 3/28/2002

Dear Sir:

Responsive to the Office Action dated November 28, 2001, please amend the above-identified application as follows:

IN THE CLAIMS - (marked-up version):

17. (amended) The apparatus of Claim 6, wherein said synchronizing circuit ensures that only one of said first and second processors utilizes said memory circuit for coupling said local memory of said first processor to said local memory of said second processor, at any one time.